

REMARKS

The Examiner objected to the Abstract, and suggested deleting the phrase: “, and associated method of formation,” from the Abstract. In response, Applicants have deleted said phrase from the Abstract.

The Examiner rejected claims 28-31, 33, 35-41, 51-54, 56, and 58-64 under 35 U.S.C. §103(a) as allegedly being unpatentable over DiStefano et al. (US 5,558,928) in view of Noddin et al. (US 5,276,955).

The Examiner rejected claims 42-44 under 35 U.S.C. §103(a) as allegedly being unpatentable over DiStefano et al. (US 5,558,928) in view of Noddin et al. (US 5,276,955).

The Examiner rejected claim 49 under 35 U.S.C. §103(a) as allegedly being unpatentable over DiStefano et al. (US 5,558,928) in view of Noddin et al. (US 5,276,955), and further in view of Koontz et al. (US 6,181,004).

Applicants respectfully traverse the §103 rejections with the following arguments.

35 U.S.C. §103(a): Claims 28-31, 33, 35-41, 51-54, 56, and 58-64

The Examiner rejected claims 28-31, 33, 35-41, 51-54, 56, and 58-64 under 35 U.S.C. §103(a) as allegedly being unpatentable over DiStefano et al. (US 5,558,928) in view of Noddin et al. (US 5,276,955).

Applicants respectfully contend that claims 28 and 51 are not unpatentable over DiStefano in view of Noddin, because DiStefano in view of Noddin does not teach or suggest each and every feature of claims 28 and 51. For example, DiStefano in view of Noddin does not teach or suggest the following features of claim 28: "a complex power-signal (CPS) substructure that has passed an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance" and "a first multilevel conductive via through the DM laminate, wherein the first multilevel conductive via is electrically coupled to a first metal layer of the CPS substructure." Similarly, DiStefano in view of Noddin does not teach or suggest the following features of claim 51: "a complex power-signal (CPS) substructure" and "a first multilevel conductive via through the DM laminate, wherein the first multilevel conductive via is electrically coupled to a first metal layer of the CPS substructure".

Applicants respectfully contend that DiStefano does not teach or suggest a CPS substructure, which the Examiner has acknowledged. The Examiner argues: "Noddin discloses 14 and 16 are complex power-signal and they are connected a conductor via as shown in Fig. 6 to conductive structures mounted to 18. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify DiStefano by the substructure is a complex

power-signal and the first metal layer is a complex power-signal, as taught by Noddin, for the purpose of providing complex power-signal to an electronic component mounted on the interposer”.

In response, Applicants find the preceding argument by the Examiner is not reasonably intelligible to one of ordinary skill in the art. For example, the phrase “is a complex power-signal and the first metal layer is a complex power-signal” has no subject and Applicants cannot ascertain the relevance of said phrase. Additionally, “the substructure” has no antecedent basis in the phrase “to modify DiStefano by the substructure ... as taught by Noddin. That is, the Examiner has not identified “a substructure” in Noddin and Applicants have no clue as to what substructure in Noddin the Examiner is referring to. The only structures in Noddin mentioned by the Examiner’s argument are a power layer 14, a signal pair layer 16, a pad layer 18, a conductor via, and conductive structures mounted to pad layer 18, and none of said structures in Noddin is a CPS substructure. Therefore, the Examiner has not identified a CPS substructure disclosed by Noddin, wherein said substructure could be used to modify DiStefano. Accordingly, Applicants contend that the Examiner has not established a *prima facie* case of obviousness in relation to claims 28 and 51.

In addition, Applicants do not understand how the Examiner envisions the modification of DiStefano’s overall structure through addition of a CPS substructure. Does the added CPS substructure replace an existing interposer? Is the added CPS substructure inserted between a circuit panel and an interposer? Applicant respectfully requests that the Examiner express specifically how DiStefano’s overall structure is modified by addition of a CPS substructure, so that both the Examiner and Applicants can objectively evaluate whether the modification is

09/24,204

24

obvious.

Additionally, the Examiner's argument of "providing complex power-signal to an electronic component mounted to the interposer" is not persuasive, since all circuit panels in DiStefano's configuration of FIG. 2 are conductively coupled to either end of the configuration. Thus, any electrical signal may be passed into the configuration at either end and received at any circuit panel within the configuration without any modification by Noddin.

Applicants next present an independent analysis to demonstrate that it is not obvious to modify DiStefano by Noddin. If DiStefano discloses a DM laminate 10b as alleged by the Examiner and if Noddin discloses a CPS substructure (assumed for argumentation purposes but not admitted), then Applicants assert that said CPS substructure from Noddin can only be combined with the DM laminate 10b of DiStefano if the alternating pattern of circuit panels 10 and interposers 12 is disturbed, which will destroy the DiStefano invention. In particular, DiStefano discloses in col. 4, line 57 - col. 5, line 9:

"A method according to this aspect of the invention preferably includes the step of stacking the circuit panels and interposers in superposed relation so that each interposer is disposed between two circuit panels, with the major surfaces of the interposers and circuit panels confronting one another, and with interconnect locations on the confronting surfaces of the circuit panels and interposers being aligned with one another. The method most preferably further includes the step of causing the flowable dielectric material to flow and conform to the major surfaces of the circuit panels. The method desirably includes the step of causing the flowable dielectric

material to flow and conform to the major surfaces of the circuit panels and on the interposers into continuous electrical conductors extending between adjacent circuit boards at their respective interconnect locations. Most preferably, the flowable dielectric and flowable conductive materials are caused to flow concomitantly with one another in a single step involving application of heat and pressure to the stacked circuit panels and interposers" (emphasis added).

Applicants contend that the preceding quote from DiStefano makes it clear that the alternating pattern of circuit panels and interposers is an essential aspect of the DiStefano invention and cannot be modified. For example, it is critical in DiStefano that "each interposer is disposed between two circuit panels, with the major surfaces of the interposers and circuit panels confronting one another" so that the flowable dielectric material will flow and conform to the major surfaces of the circuit panels, and so that the flowable dielectric material flows and conforms to the major surfaces of the circuit panels. This principle underlying the DiStefano invention is repeated throughout the DiStefano disclosure and in the DiStefano claims. For example, see claim 1 of DiStefano. Thus, Applicants maintain that to add a CPS substructure into the structural configuration of DiStefano will disable the preceding relationship between the circuit panels and the interposers such that the DiStefano invention will be effectively destroyed.

Applicants also note that DiStefano in view of Noddin does not teach or suggest the following feature of claim 28: "a complex power-signal (CPS) substructure that has passed an electrical performance acceptance test ". The Examiner's argument that "DiStefano discloses

testing the substructures" is not persuasive, since claim 28 requires testing a CPS substructure and DiStefano does not teach or suggest a CPS substructure as admitted by the Examiner. Distefano discloses testing only circuit panels and interposers.

Based on the preceding arguments, Applicants respectfully maintain that claims 28 and 51 are not unpatentable over DiStefano in view of Noddin, and that claims 28 and 51 are in condition for allowance. Since claims 29-31, 33, 35-41, and 63-64 depend from claim 28, Applicants contend that claims 29-31, 33, 35-41, and 63-64 are likewise in condition for allowance. Since claims 52-54, 56 and 58-62 depend from claim 51, Applicants contend that claims 52-54, 56 and 58-62 are likewise in condition for allowance.

Applicants note that many of the dependent claims have an independent basis for patentability. For example, claims 29 and 52 recite: "wherein the first multilevel conductive via is a stacked via". The Examiner's allegation that via 26b in FIG. 2 of DiStefano is a stacked via is incorrect, because a stacked via is characterized by "discontinuities in sidewall smoothness at layer interfaces", which is not satisfied by via 26b in FIG. 2 of DiStefano. See Applicants' specification, page 8, lines 19-21.

As another example, claims 38 and 61 recite: "a conducting via beginning at the first external surface of the CPS substructure and extending through a fraction of a total thickness of the CPS substructure", and claims 39-41 and 62-64 recite limitations on said "fraction". Applicants contend that the Examiner's arguments relating to vias 26, 26b, and 26c are irrelevant, since vias 26, 26b, and 26c are not vias of a CPS structure as required by claims 38-41

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and 61-64.

09/924,204

28

35 U.S.C. §103(a): Claims 42-44

The Examiner rejected claims 42-44 under 35 U.S.C. §103(a) as allegedly being unpatentable over DiStefano et al. (US 5,558,928) in view of Noddin et al. (US 5,276,955).

Applicants respectfully contend that claim 42 is not unpatentable over DiStefano in view of Noddin, because DiStefano in view of Noddin does not teach or suggest each and every feature of claim 42. For example, DiStefano in view of Noddin does not teach or suggest the following features of claim 42: "a complex power-signal (CPS) substructure that has satisfied an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance, a first dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2, and wherein a first multilevel conductive via through the first DM laminate is electrically coupled to a first metal layer of the CPS substructure", based on the same reasons presented *supra* in conjunction with claim 28.

In addition, DiStefano in view of Noddin does not teach or suggest "a second dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on a second external surface of the CPS substructure, wherein M is at least 2, and wherein a second multilevel conductive via through the second DM laminate is electrically coupled to a second metal layer of the CPS substructure".

09/924,204

29

The Examiner argues: "DiStefano/Noddin fail to disclose providing another DM laminate to the opposite side of the CPS substructure. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide another DM laminate, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8. Further, it would have been obvious to one having ordinary skill in the art at the time the invention was made to position another DM laminate to the opposite side of the CPS substructure, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70."

Applicants respectfully contend that the preceding argument by the Examiner is not legally persuasive, because the Examiner has inaccurately stated the holdings in *St. Regis Paper* and *In re Japikse*. In addition, the Examiner has not applied *St. Regis Paper* and *In re Japikse* to the pertinent aspects of claim 42 in accordance with acceptable standards of legal analysis. In the absence of credible legal analysis by the Examiner, the preceding argument by the Examiner is not legally persuasive. Accordingly, Applicants respectfully contend that the Examiner has not established a *prima facie* case of obviousness in relation to claim 42.

In addition, "to position another DM laminate to the opposite side of the CPS substructure", as argued by the Examiner, would disturb the relationship between the circuit panels and the interposers so as to destroy the DiStefano invention, as explained *supra*.

Based on the preceding arguments, Applicants respectfully maintain that claim 42 is not unpatentable over DiStefano in view of Noddin, and that claim 42 is in condition for allowance. Since claims 43-44 depend from claim 42, Applicants contend that claims 43-44 are likewise in

condition for allowance.

Applicants also note that the Examiner has not presented any argument relating to claim 43. Accordingly, Applicants respectfully contend that the Examiner has failed to establish a *prima facie* case for obviousness in relation to claim 43.

35 U.S.C. §103(a): Claim 49

The Examiner rejected claim 49 under 35 U.S.C. §103(a) as allegedly being unpatentable over DiStefano et al. (US 5,558,928) in view of Noddin et al. (US 5,276,955), and further in view of Koontz et al. (US 6,181,004).

Applicants respectfully contend that claim 49 is not unpatentable over DiStefano in view of Noddin, and further in view of Koontz, because DiStefano in view of Noddin, and further in view of Koontz does not teach or suggest each and every feature of claim 49. For example, DiStefano in view of Noddin, and further in view of Koontz does not teach or suggest "a complex power-signal (CPS) substructure that has passed an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and erroneous an impedance; a first dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2, and wherein a first multilevel conductive via through the first DM laminate is electrically coupled to a first metal layer of the CPS substructure", based on the same

09/924,204

31

reasons presented *supra* in conjunction with claim 28.

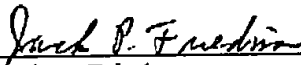
In addition, DiStefano in view of Noddin does not teach or suggest "a second dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on a second external surface of the CPS substructure, wherein M is at least 2, and wherein a second multilevel conductive via through the second DM laminate is electrically coupled to a second metal layer of the CPS substructure", based on the same reasons presented *supra* in conjunction with claim 42.

Based on the preceding arguments, Applicants respectfully maintain that claim 49 is not unpatentable over DiStefano in view of Noddin, and further in view of Koontz, and that claim 49 is in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below.

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